

IN THE DRAWINGS:

In response to the Office Action, a Replacement Figure 7 which corrects the last reference numeral to read "710" is attached.

**REMARKS**

Claim 3 is amended by hereby. No claims are canceled or added. Accordingly, claims 1-36 remain pending. Claims 17-36 are withdrawn from consideration.

In the Office Action dated March 1, 2005, the Examiner repeated the verbal Restriction Requirement relayed to the Applicant on February 8, 2005. Specifically, the Examiner noted that the application contains two patentably distinct groups of invention: (1) Group I, encompassing claims 1-16, drawn to a method of processing a layer containing a high-permittivity material in a plasma processing system, and (2) Group II, encompassing claims 17-36, drawn to a plasma processing system. The Applicant affirms the election of Group I hereby, without traverse.

In the Office Action, the Examiner objected to the drawings under 37 C.F.R. § 1.84(p)(4), stating that the reference number “708” in Fig. 7 has been used to designate both the first and last steps in the flowchart. The Examiner correctly noted that paragraph [0051] of the specification relies on reference number “710” to refer to the last step. To address the Examiner’s objection, the Applicant supplies herewith a replacement Fig. 7. “710” now designates the last step in the flowchart. Accordingly, the Applicant respectfully requests that the Examiner withdraw the objection to the drawings.

The Examiner also objected to the specification under 37 C.F.R. § 1.75(d)(1) and M.P.E.P. § 608.01(o). Specifically, the Examiner stated that the specification fails to provide proper antecedent basis for the feature recited by claim 3 “modifying partially dissociates the layer containing the high-permittivity material.” While the Applicant respectfully disagrees with the Examiner, the Applicant presents an amendment to claim 3 that the Applicant believes addresses the Examiner’s objection.

Specifically, the Applicant has amended claim 3 to recite that the modifying disrupts the atomic structure of the layer containing the high-permittivity material. Support for this feature may be found in paragraph [0025], for example. In view of this change, the Applicant respectfully requests that the Examiner withdraw the objection to the specification.

In the Office Action dated March 1, 2005, the Examiner rejected claims 1-4, 6-10, 15, and 18 under 35 U.S.C. § 102(e) as anticipated by Yu et al. (U.S. Patent No. 6,818,553). The Applicant respectfully disagrees with this rejection and, accordingly, traverses same. The Applicant respectfully submits that Yu et al. does not describe each and every feature recited by the claims and, therefore, cannot anticipate the claims.

Yu et al. describes an etching process for high-k gate dielectrics. To understand the etching process discussed by Yu et al., it is first helpful to understand the structure upon which Yu et al. operates. As shown in Fig. 1 of Yu et al., reproduced below, the structure 10 includes a silicon substrate with shallow trench isolation structures 12. (Yu et al. at col. 2, lines 17-23.) A high-k dielectric layer 14 overlays the silicon substrate 10. (Yu et al. at col. 2, lines 24-26.) A gate layer 16 is formed over the dielectric layer 14. (Yu et al. at col. 2, lines 30-31.) The gate layer 16 interacts with the high-k dielectric layer 14 to form an interfacial layer 18, which is hard to etch. (Yu et al. at col. 2, lines 40-42.) A gate anti-reflective coating 20 (“ARC”) is deposited over the gate layer 16. (Yu et al. at col. 2, lines 52-54.)

Fig. 2 illustrates the cross-section of the ARC 20 and poly-Si gate layer 16 after being patterned. (Yu et al. at col. 2, lines 52-54.) The patterned ARC 20' and the patterned poly-Si gate 16' are then subject to further processing. In particular, as

illustrated in Fig. 3, the patterned ARC 20 is stripped from the patterned poly-Si gate 16'. (Yu et al. at col. 2, lines 58-60.)

U.S. Patent Nov. 16, 2004 Sheet 1 of 3 US 6,818,553 B1

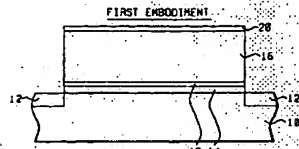


FIG. 1

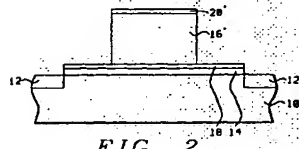


FIG. 2

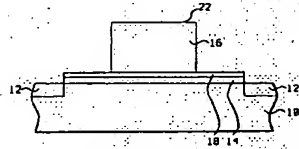


FIG. 3

U.S. Patent Nov. 16, 2004 Sheet 2 of 3 US 6,818,553 B1

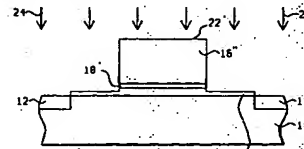


FIG. 4

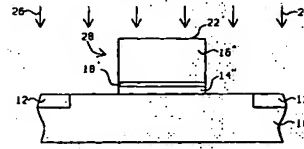


FIG. 5

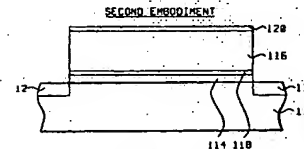


FIG. 6

Fig. 4 of Yu et al. illustrates an argon (Ar) sputter or fluorine (F)-based-chemistry plasma etch 24 which thins the patterned poly-Si gate layer 16' to a thinner version 16''. (Yu et al. at col. 2, lines 63-67.) The Ar sputter/F-based-chemistry etch also removes the interfacial layer 18 and a portion of the high-k dielectric layer 14 under the interfacial layer 18. (Yu et al. at col. 2, line 67, through col. 3, line 6.) As illustrated in Fig. 5, a wet etch 26 is used to remove the remaining exposed portions of the high-k dielectric layer 14' after the etch 24. (Yu et al. at col. 3, lines 48-54.)

Yu et al. does not describe two of the features recited by claim 1. Specifically, Yu et al. does not describe modifying the layer containing the high-permittivity material by exposing the layer to a plasma nor does it describe removing the modified layer. Yu et al. merely describes removing the interfacial layer 18 and removing a portion of the high-k dielectric layer 14 via Ar sputter or F-based-chemistry plasma etch 24. There is no mention of "modifying" the high-k dielectric layer.

The instant application provides insight into what is meant by “modifying”, at least in part. Specifically, as reproduced below for the Examiner’s convenience, the specification states:

[0025] The exact effect of the plasma treatment on the high-k layer is currently not known. However, the plasma treatment may increase the amorphous content of the high-k layer and possibly breaks chemical bonds that create atomic fragments in the high-k layer. In addition to using inert gases the disclosed plasma treatment can utilize reactive gases, where the ion energy is adequate to disrupt the atomic structure of the high-k layer in such a way that the subsequent wet-etching process is able to remove the modified high-k layer. When using a reactive plasma, the process conditions can be selected such that the existing gate-conductor features are not etched.

Yu et al. does not describe or suggest anything along these lines. Accordingly, the Applicant respectfully submits that Yu et al. does not describe each of the features recited by claim 1 and, as a result, cannot anticipate claim 1 or claims 2-14 that depend on claim 1. For similar reasons, claims 15 and 16 are not anticipated by Yu et al.

Claim 5 was rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over Yu et al. in view of Yang et al. (U.S. Patent No. 6,579,809). The Examiner also rejected claims 11, 12, and 14 under 35 U.S.C. § 103(a) as being unpatentable over Yu et al. in view of Ranft et al. (U.S. Patent No. 6,539,449). The Applicant respectfully disagrees with these rejections and, therefore, respectfully traverses same.

As discussed above, Yu et al. fails to describe each and every feature recited by claims 1-16. Yang et al. and Ranft et al. both fail to correct the deficiencies noted with respect to Yu et al. and, accordingly, cannot be combined properly with Yu et al. to maintain a supportable rejection against claims 1-16. Accordingly, the Applicant

respectfully requests that the Examiner withdraw the rejection of the claims under 35 U.S.C. § 103(a).

Yang et al. describes an in-situ gate etch process for fabrication of a narrow gate transistor structure with a high-k dielectric. In the exemplary embodiment, the high-k dielectric material forms the etch stop layer 62. (Yang et al. at col. 5, lines 5-9.) The high-k dielectric material 62 is removed using an etch chemistry of HBr, He, or CF<sub>4</sub>. (Yang et al. at col. 7, lines 20-27.) Yang et al. does not describe or suggest modifying the layer containing the high-permittivity material by exposing the layer to a plasma nor does it describe removing the modified. Accordingly, the Applicant respectfully submits that Yang et al. cannot be combined properly with Yu et al. to render any of the claims obvious. As a result, the Applicant respectfully requests that the Examiner withdraw the rejection.

Ranft et al. also does not assist the Examiner in fashioning a rejection of the claims. Ranft et al. describes a downstream surface cleaning process. Ranft et al., however, does not describe or suggest modifying the layer containing the high-permittivity material by exposing the layer to a plasma nor does it describe removing the modified. Accordingly, the Applicant respectfully submits that Ranft et al. cannot be combined properly with any of the remaining references to render any of the claims obvious. As a result, the Applicant respectfully requests that the Examiner withdraw the rejection.

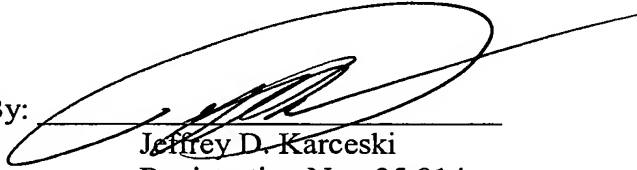
Each of the rejections asserted by the Examiner having been addressed, the Applicant respectfully submits that claims 1-16 are patentable over the references cited by the Examiner. Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejections asserted against claims 1-16 and pass this application quickly to issue.

If the Examiner believes a telephone conference would be helpful, she is invited to contact the undersigned at the telephone number given below.

Respectfully submitted,

PILLSBURY WINTHROP SHAW PITTMAN LLP

By:

A handwritten signature in black ink, appearing to read 'Jeffrey D. Karceski', is written over a horizontal line.

Jeffrey D. Karceski  
Registration No.: 35,914

P.O. Box 10500  
McLean, Virginia 22102  
(703) 905-2110  
(703) 905-2500 Facsimile

Customer No. 00909